Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for manufacturing a double-sided flexible printed board, comprising the following steps of:

(A) forming a polyimide precursor layer on a metal layer;

(B) forming an upper circuit layer on the polyimide precursor layer by a semi-additive technique, leaving the polyimide precursor layer partially exposed; and

(C) imidating the partially exposed polyimide precursor layer to form a polyimide insulating layer.

2. (Original) The method according to claim 1, wherein step (M) in which the formation of a through hole for ensuring conductivity between the metal layer and the upper circuit layer is performed between step (B) and step (C) or subsequent to step (C).

3. (New) A method for manufacturing a double-sided flexible printed board, comprising the following steps of:

(A) forming a polyimide precursor layer on a metal layer;

(B) forming an upper circuit layer on the polyimide precursor layer by a semi-additive technique; and

(C) imidating the polyimide precursor layer, while the polyimide precursor layer includes the upper circuit layer that has been formed on the polyimide precursor layer, to form a polyimide insulating layer.

4. (New) The method according to claim 3, wherein step (M) in which the formation of a through hole for ensuring conductivity between the metal layer and the upper circuit layer is performed between step (B) and step (C) or subsequent to step (C).

5. (New) A method for manufacturing a double-sided flexible printed board, comprising the following steps of:

(A) forming a polyimide precursor layer on a metal layer;

(B) forming an upper circuit layer on the polyimide precursor layer by a semi-additive technique; and

(C) after step (B), imidating the polyimide precursor layer to form a polyimide insulating layer.

6. (New) The method according to claim 5, wherein step (M) in which the formation of a through hole for ensuring conductivity between the metal layer and the upper circuit layer is performed between step (B) and step (C) or subsequent to step (C).